Conversion de puissance directe avec faible distorsion de courant d'entrée pour un système multimoteur

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RÉSUMÉ

Implementation of an effective solution in Adjustable Speed Drive (ASD), for reduction of Total Harmonic Distortion (THD) level in input line current, is currently the object of many efforts of scientists and engineers in power electronics.

In this thesis, a popular converter structure, two-stage Direct Power Electronic Converter (DPEC), and a popular control strategy, Space Vector Modulation (SVM), are presented as an effective solution for ASDs.

The solution has been simulated in the real-time simulation environments Xilinx System Generator™ (XSG™) and RT-LAB™. The results show an effective reduction of the THD level in input line current and output voltage, sinusoidal input/output, with respect to other current solutions.

Hardware Design Language (HDL) codes are generated according to the control algorithm applied for the PWM pattern generation. HDL codes are analyzed for the purpose of FPGA implementation, because of FPGAs' higher solution speed and capability in the mathematical complex equations than microcontrollers.

The result of codes synthesis, with Leonardo Spectrum software, is presented and an appropriate FPGA, with correspondent capacity and code volume, is selected.

As the result of this research, simulations of this solution in two real-time workshops and HDL codes generation with synthesis have been realised.